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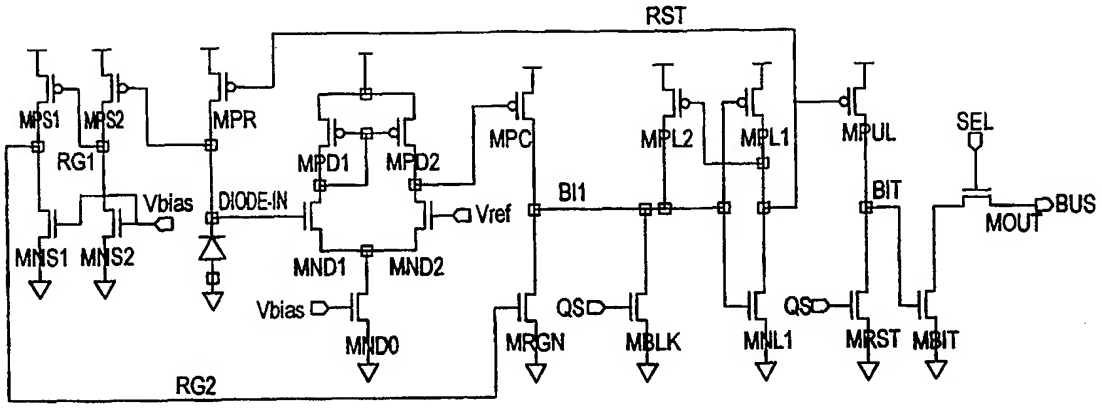

(57) Abstract

An asynchronous mode sigma–delta modulator circuit is usable, for example, at each pixel of a CMOS image sensor. The asynchronous sigma–delta modulator includes a comparator circuit (MND0, MND1, MND2, MPD1, MPD2) whose output switches to indicate when an input signal has reached a predetermined reference level, and a latch circuit (MNL1, MPL2, MPL2) that asserts a pulse signal when the comparator output switches. A pulse capture circuit (MPUL, MRST, MBIT) senses the pulse signal and stores it as a logic value until sampled by a clocked output circuit. Regeneration circuitry (MPS1, MNS1, MPS2, MNS2, MRGN) resets the input signal and the latch circuit after the pulse signal is captured by the pulse capture circuit.

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TITLE OF THE INVENTION

An Asynchronous Mode Pixel-Parallel Sigma-Delta A/D Converter for CMOS Imagers

CROSS REFERENCE TO RELATED APPLICATIONS

This application claims priority under 35 U.S.C. §119(e) of U.S. provisional patent application no. 60/077,760, filed March 12, 1998, entitled "An Asynchronous Mode Pixel-Parallel Sigma-Delta A/D Converter for CMOS Imagers."

STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT

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BACKGROUND OF THE INVENTION

On-chip analog-to-digital (A/D) conversion has been recognized as a desirable feature for CMOS image sensors, because it can reduce power and increase system integration. To date several image sensors have been developed with column-parallel A/D conversion, such as a single-slope sensor architecture, a successive approximation architecture, and a second-order current-mode sigma-delta architecture. These designs typically require a significant amount of area and careful layout, because the pitch of the A/D converters must be matched to that of the sensor columns.

In order to build compact, portable low-power devices for real-time image processing, it is useful to provide more

integration and parallelism for on-chip computations. The architecture which is most appropriate for pixel-parallel A/D conversion is a first-order sigma-delta loop, because it can be implemented in a very small area and computations can be performed on the bit stream output before decimation with simple logic circuits.

A block diagram of a first-order sigma-delta modulator is illustrated in Figure 1. With x_i representing the sampled input data at time t=iT, T being the sampling period, and y_i representing the binary-valued output of the modulator, it can be shown that

$$y_i = x_{i-1} + e_i - e_{i-1} \quad (1)$$

where e_i is the quantization error at step i. If the sequence y_i is optimally filtered and decimated down to the Nyquist rate $2f_o$ of the input, the remaining in-band noise is given by

$$n_o(dB) = \bar{e} + 5.2 - 9\log_2 N \quad (2)$$

where N is the oversampling ratio, $N = (2f_0T)^{-1}$, and $\bar{e}$ is the root mean square quantization error from the loop A/D. This equation implies that one can ideally obtain 1.5 bits of resolution for every doubling of N. Many algorithms have been developed over the last three decades for recovering high resolution (multi-bit) data from sigma-delta output streams. These can be readily implemented on a digital signal processor interfaced to the imager.

Pixel-parallel sigma-delta A/D converter designs developed for 2D CMOS imagers are known in the art. One design is described by Boyd Fowler in his 1995 Ph.D. thesis entitled "CMOS Area Image Sensors with Pixel Level A/D

Conversion," and also in corresponding U.S. Patent No. 5,461,425. Another design is described by Yang et al in "A 128 X 128 Pixel CMOS Area Image Sensor With Multiplexed Pixel Level A/D Conversion," Digest of Technical Papers, Custom Integrated Circuits Conference, 1996. These designs employ a classical synchronous architecture. In particular, these designs are based on a clocked comparator and a switched-capacitor circuit implementing the 1-bit D/A converter in the feedback loop.

BRIEF SUMMARY OF THE INVENTION

In accordance with the present invention, an asynchronous sigma-delta modulator is disclosed that oscillates at a rate proportional to an input light value, generating a regular stream of pulses that is sampled at a rate f_s (=1/T) to produce a binary output data stream. The asynchronous architecture requires a minimal number of analog components and thus can be operated at high sampling rates with little signal-to-noise ration (SNR) degradation. The architecture has been demonstrated to operate with measured SNR of 60 dB at an equivalent frame rate of 5000 frames/second (312.5 kHz pixel sampling rate). At moderate rates such as 30 frames/second, a circuit implementation of the architecture is capable of measuring light intensities over more than 120 dB dynamic range. The asynchronous design also minimizes the number of analog components that must be well matched in order to reduce fixed pattern noise, and it allows greater control of the sensitivity and frame rate of the imager.

An embodiment of the asynchronous sigma-delta modulator is disclosed that includes a comparator circuit whose output switches to indicate when an input signal has reached a predetermined reference level, and a latch circuit that

asserts a pulse signal when the comparator output switches. A pulse capture circuit senses the pulse signal and stores it as a logic value until sampled by a clocked output circuit. Regeneration circuitry resets the input signal and the latch circuit after the pulse signal is captured by the pulse capture circuit.

Other aspects, features, and advantages of the present invention are disclosed in the detailed description that follows.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING

Figure 1 is a block diagram of a canonical first-order sigma-delta modulator circuit for sampled data as is known in the prior art;

Figure 2 is a waveform diagram illustrating the different output waveforms generated by synchronous and asynchronous modulator circuits;

Figure 3 is a schematic diagram of an asynchronous first-order sigma-delta A/D converter cell in accordance with the present invention;

Figure 4 (consisting of Figures 4a, 4b and 4c) is a timing diagram of several signals in the circuit of Figure 3;

Figure 5 is a plot of the pixel output of the sigma-delta converter cell of Figure 3 as a function of sampling period T for constant illumination; and

Figure 6 is a plot of the output of the sigma-delta converter cell of Figure 3 as a function of illumination at a 5 kHz sampling rate.

DETAILED DESCRIPTION OF THE INVENTION

Figure 2 illustrates the outputs of both an asynchronous modulator circuit (solid line) and a

synchronous modulator circuit (dashed line) assuming a constant input value x. These waveforms are based on a continuous-time version of the first order circuit of Figure 1 in which the accumulator is replaced with an integrator and the variables are continuous functions of time. The asynchronous modulator generates a bit stream output that is equivalent to the output of the synchronous modulator. This equivalence was first observed by Candy and Benjamin in a paper entitled "The Structure of Quantization Noise from Sigma-Delta Modulation," IEEE Transactions on Communications, vol. 29(9), pages 1316-1323 (1981).

With reference to Figure 2, it is assumed that the input x is a negative quantity, so that the integrator output, ω, decreases with time. When the sampled value of ω is less than or equal to the reference level B in the synchronous modulator (dashed line), a '1' is output, and the circuit is reset. As part of the resetting, an impulse of $|x_{max} \cdot T|$ is added back to the input, where T is the clock period. The comparison between the integrator output and the reference B is synchronized with the clock edge, so that ω typically drops a variable amount below B before the circuit is reset. The high reference level A, which is equal to $B + |x_{max} \cdot T|$, represents the maximum value of ω.

When the integrator output reaches B in the asynchronous modulator (solid waveform), the circuit is immediately reset to the fixed level A. At the same time, a pulse is generated that is sampled on the next clock edge to produce the output bit.

The key observation in the waveforms of Figure 2 is that when the synchronous modulator resets, its waveform rejoins that of the free running asynchronous circuit, and hence the bit stream outputs of the two are identical. The

asynchronous modulator oscillates with period $(x_{max}/x)\cdot T$, and thus the average value of the output converges to x/x_{max}.

The primary advantage of the asynchronous modulator is that it is reset to a fixed level when its output level ω drops to B. This is in contrast to the synchronous modulator, which requires that an accurate analog value be added back to the output upon reset. This feature of the asynchronous modulator eliminates the problem of mismatch in analog components, which is a major source of fixed pattern noise when synchronous cells are implemented in an array.

Figure 3 shows a schematic of an asynchronous modulator cell suitable for use in a CMOS imager with photodiode input. The circuit is composed of four sections:

1. A differential amplifier/comparator formed of transistors MND0, MND1, MND2, MPD1, and MPD2. This circuitry continuously tests whether the photodiode voltage DIODE_IN has dropped below an assigned reference level V_{ref}.
2. A fast path bistable circuit consisting of transistors MNL1, MPL1 and MPL2 along with set and reset transistors MPC, MRGN, and MBLK. This circuit generates a reset pulse RST for transistor MPR that brings the photodiode voltage DIODE_IN back to its initial high level after switching of the comparator has been detected.
3. A slow path regeneration circuit consisting of the pair of common-source amplifiers MPS1-MNS1 and MPS2-MNS2. This circuit controls a transistor MRGN to turn off the reset pulse RST to allow a new integration cycle to proceed.
4. A pulse capture circuit including transistors MPUL, MRST, and MBIT. This circuit senses and stores the reset pulse RST as a signal BIT until it is sampled by a

clocked output circuit. A transistor MOUT connected to a row select signal SEL gates the cell output onto a column bus used to read the pixel bit stream in a 2D array layout.

The operation of the circuit of Figure 3 is now described with additional reference to the timing diagrams of Figure 4. It should be noted that the time span in Figures 4a and 4b is approximately 200 microseconds, whereas Figure 4c is an expanded view of a 1.6 microsecond interval showing the relationship among several signals involved in reading the pixel value.

During most of each period of oscillation, the reset transistor MPR is turned off, and the diode photocurrent passively reduces the voltage DIODE_IN on the capacitance at the gate of MND1 from a value of approximately 3 volts to a lower voltage V_{ref}. Before the signal DIODE_IN reaches V_{ref}, however, it first passes through a value that is a threshold voltage below V_{DD}. When it does so, the transistor MPS2 is turned on, causing the signal RG1 to rise and the signal RG2 to fall. The signal RG2 reaches a value sufficient to turn off the regeneration transistor MRGN before the signal DIODE_IN reaches the reference level V_{ref}. As shown in the timing diagrams, in the illustrated embodiment this occurs approximately 20 microseconds before the signal DIODE_IN reaches V_{ref}. The timing is influenced by various aspects of the circuit including the value of the reference level V_{ref}, and may be different in alternative embodiments.

Once the signal DIODE_IN reaches V_{ref}, the comparator output quickly drops below V_{DD}, turning on transistor MPC and raising its drain voltage BI1 towards V_{DD}. The positive feedback of the cross-coupled PMOS transistors in the half-latch MPL1-MNL1-MPL2 quickly yanks the voltage BI1 to the

positive rail and forces the signal RST at the output of the inverter pair MPL1-MNL1 to ground. This assertion of the signal RST turns on both the reset transistor MPR and the pulse capture transistor MPUL.

When MPR is conducting, the diode voltage DIODE_IN and the comparator output are returned to V_{DD}, and the transistor MPC is turned off. The high diode voltage DIODE_IN also causes the signal RG1 in the two-stage common-source amplifier pair, MPS1-MNS1 and MPS2-MNS2, to switch slowly from V_{DD} to GND. When the signal RG1 falls to a threshold below V_{DD}, the output RG2 of the second stage (MPS1-MNS1) switches high rapidly. This in turn causes the regeneration transistor MRGN to conduct, resetting the latch and turning off both transistors MPR and MPUL.

The differential pair and the common-source amplifiers are biased in the weak inversion region to reduce power and maximize gain. Because of the low level of current driven by the bias transistors MNS1 and MNS2, the common-source amplifiers have a slow fall time and fast rise time. Therefore, the time to propagate a transition from the input to the output of the regeneration circuit is long enough to ensure that the diode voltage DIODE_IN is fully reset to its initial high level before MPR is turned off. Because of the high gain and fast rise of the second stage, the low-to-high transition is very abrupt once the signal RG1 reaches the trip point, roughly $V_{DD}-V_{TH}$. This operation minimizes the time that the input latch might be held at an intermediate level, which would burn static power.

The pulse capture circuit is read and reset once every clock period using the signals PC, SEL and QS. If the oscillator resets during the time between two reads, MPUL turns on and a high value is stored on the gate of MBIT.

During a read operation, the output bus (signal BUS) is first precharged to a high level by precharge circuitry (not shown) responsive to the signal PC. During the next clock cycle, the signal SEL is asserted. The bus is then discharged or not depending on the state of MBIT. After the bit is read, the signal SEL is brought low and the signal QS is brought high to reset the gate of MBIT to GND.

The signal QS is also applied to a blocking transistor MBLK used to prevent a pulse from occurring while the output is being reset by blocking the reset latch. It also serves to refresh the latch input from leakage due to MPC that might otherwise cause premature switching during a long integration time. It should be noted, however, that the blocking transistor is an optional component that may be omitted in alternative embodiments.

In order to build a CMOS imager, the pixels described above are arranged in a regular grid of rows and columns. A row decoder, designed with standard methods, is used to sample one row of the array at a time. Clock signals SEL and QS as described above are gated through the decoder onto the chosen row. The pixels in each column of the array share a single bus line, which is driven by the pixel in the addressed row. At the top of each column a standard circuit is used to precharge the bus line, which the pixel may or may not pull down depending on its state, and to latch the output bit. A multiplexer is used to gate groups of column outputs, stored in the latches, onto output pins. Either or both of the row and column addresses may be supplied externally or generated on-chip using counters or other address-generating circuitry. The data is collected in a high-speed external memory, which is subsequently read into a computer for analysis. Arrays of up to 64 x 64 pixels

have been fabricated, but there are no known technical impediments to realizing larger arrays.

Figures 5 and 6 illustrate some performance aspects of the sigma-delta A/D converter circuit of Figure 3. Figure 5 illustrates the linear response of the pixel to changes in the sampling clock period, T, from 3.2 microseconds to 100 microseconds (corresponding to a range of sampling rates from 312.5 kHz to 10 kHz). Figure 5 shows that the sigma-delta decimated and low-pass-filtered output, expressed as a fraction of saturation, is directly proportional to T, as it should be. Notably, there is no noticeable distortion at sampling rates over 300 kHz. The observed deviations in the measured values from the best line fit are attributed to variations in the light source intensity over the course of the experiment. The measured SNR at 312.5 kHz was greater than 60 dB in mid-range.

Figure 6 shows that the pixel response is also a linear function of incident illumination. The data in Figure 6 were gathered using a sampling rate of 5 kHz and a calibrated monochromatic light source having a wavelength of 600 nm. The slope of the line is related to the conversion gain of the photodiode, the value of the reference level V_{ref}, and the sampling rate. It is estimated that this circuit has the potential for acquiring images with over 120 dB dynamic range with the appropriate combination of these parameters.

It will be apparent to those skilled in the art that modification to and variation of the above-described methods and apparatus are possible without departing from the inventive concepts disclosed herein. Accordingly, the invention should be viewed as limited solely by the scope and spirit of the appended claims.

CLAIMS

What is claimed is:

1. A sigma-delta analog-to-digital converter, comprising:

an oscillator operative in response to an input analog value to independently oscillate between two signal levels having predetermined separation such that the oscillation frequency has a known relationship with respect to the input analog value; and

sampling circuitry operative to sample the oscillator at a known rate above the oscillation frequency to provide a binary output signal from which the analog value can be derived.

2. An asynchronous sigma-delta analog-to-digital converter, comprising:

a comparator operative to provide a comparator output signal indicating whether an input signal has reached a predetermined reference level;

a latch circuit operative to assert a pulse signal upon assertion of the comparator output signal;

a pulse capture circuit operative to sense the pulse signal and store a corresponding logic value until sampled by a clocked output circuit; and

regeneration circuitry operative in response to the pulse signal to (i) reset the input signal to an initial level such that the comparator output signal becomes deasserted, and (ii) reset the latch circuit and deassert the pulse signal after sensed by the pulse capture circuit, the regeneration circuitry being further operative to (i) enable an external device to control the value of the input signal in the absence of the pulse signal and (ii) enable

the setting of the latch circuit and assertion of the pulse signal as the input signal approaches the reference level.

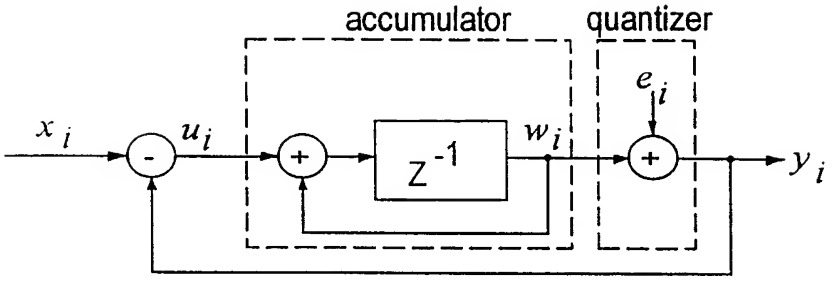

FIG. 1

(PRIOR ART)

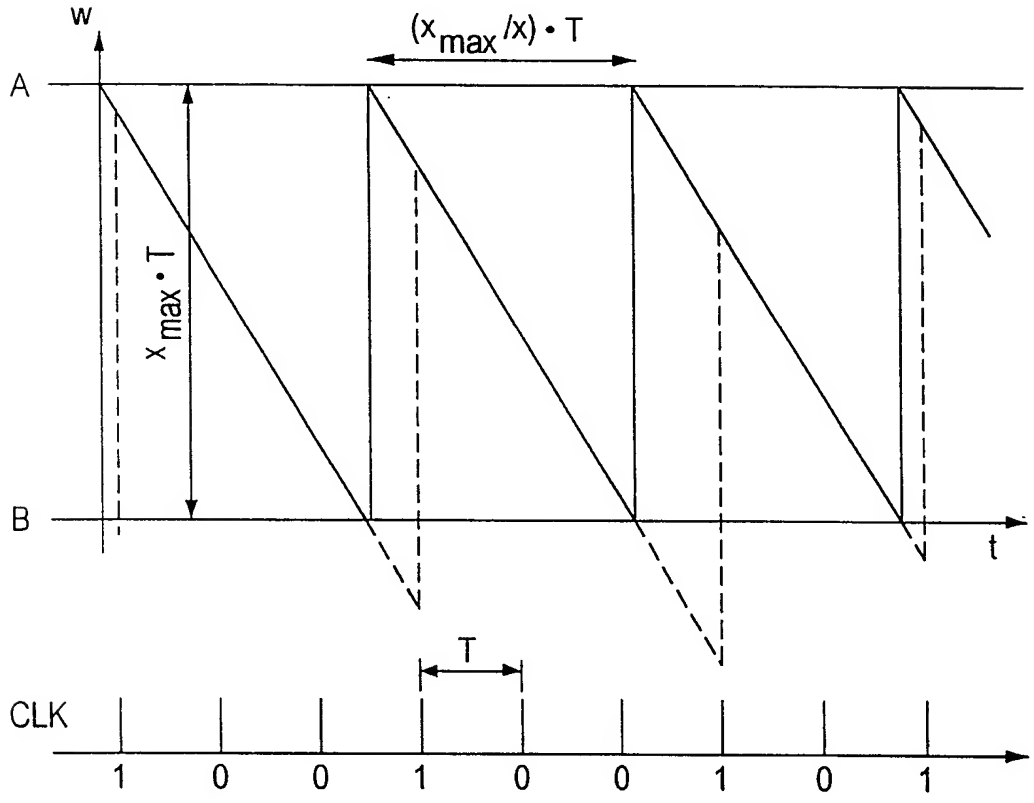

FIG. 2

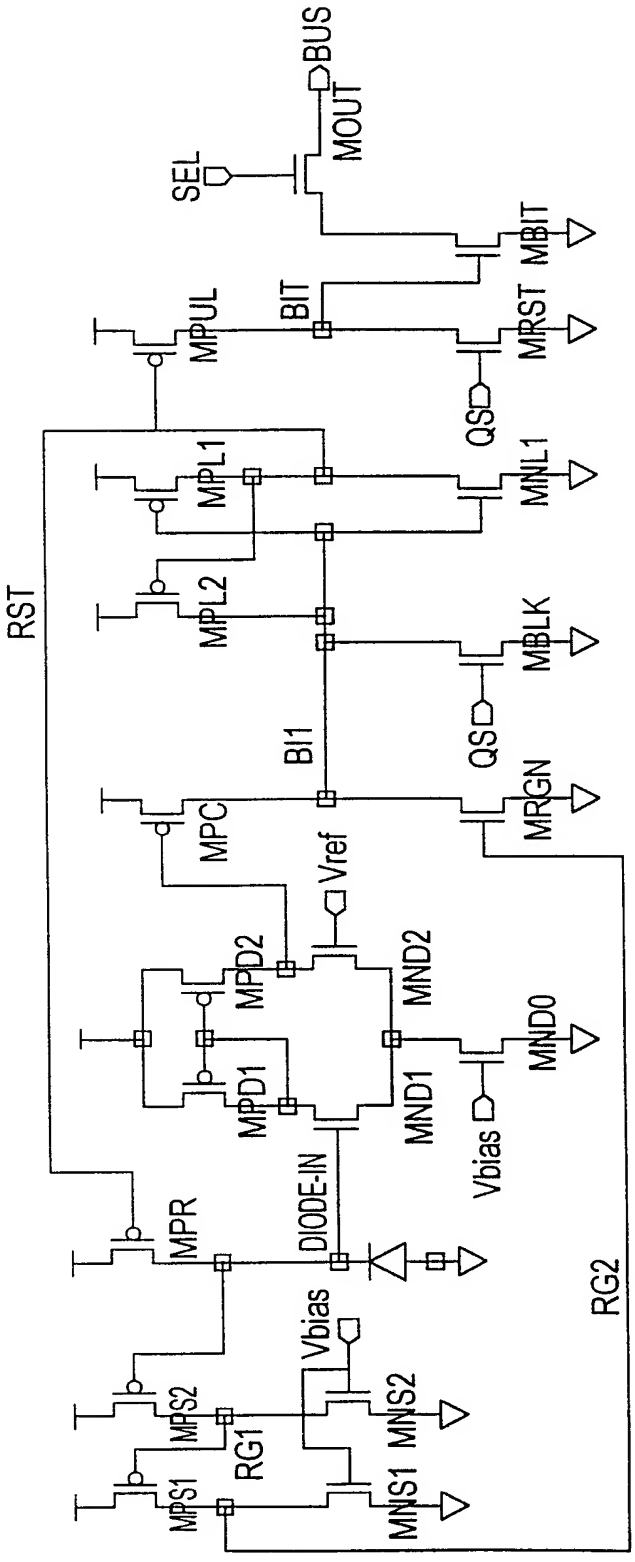
BUS
MOUT
SEL
MBIT
MRST
MPUL
BIT
QS
MNL1
MPL1
MPL2
MBLK
RST
BI1
QS
MRGN
MPC
Vref
MPD2
MND2
MND0
MPD1
MND1
Vbias
DIODE-IN
MPR
RG2
Vbias
MPS2
MNS2
RG1
MPS1
MNS1

FIG. 3

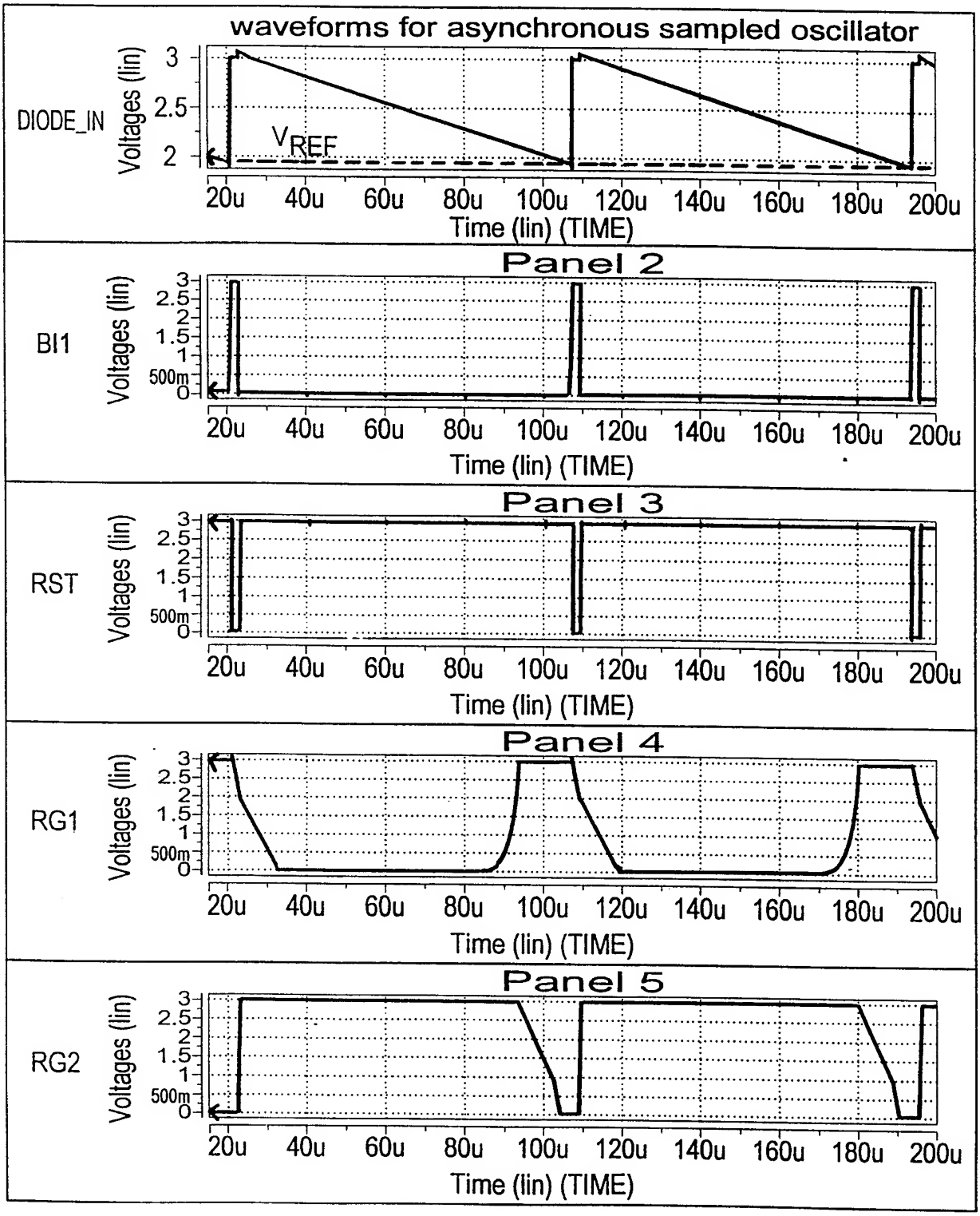
waveforms for asynchronous sampled oscillator
DIODE_IN
Voltages (lin)
3
2.5
2
V_{REF}
20u 40u 60u 80u 100u 120u 140u 160u 180u 200u
Time (lin) (TIME)
Panel 2
BI1
Voltages (lin)
3
2.5
2
1.5
1
500m
0
20u 40u 60u 80u 100u 120u 140u 160u 180u 200u
Time (lin) (TIME)
Panel 3
RST
Voltages (lin)
3
2.5
2
1.5
1
500m
0
20u 40u 60u 80u 100u 120u 140u 160u 180u 200u
Time (lin) (TIME)
Panel 4
RG1
Voltages (lin)
3
2.5
2
1.5
1
500m
0
20u 40u 60u 80u 100u 120u 140u 160u 180u 200u
Time (lin) (TIME)
Panel 5
RG2
Voltages (lin)
3
2.5
2
1.5
1
500m
0
20u 40u 60u 80u 100u 120u 140u 160u 180u 200u
Time (lin) (TIME)

FIG. 4a

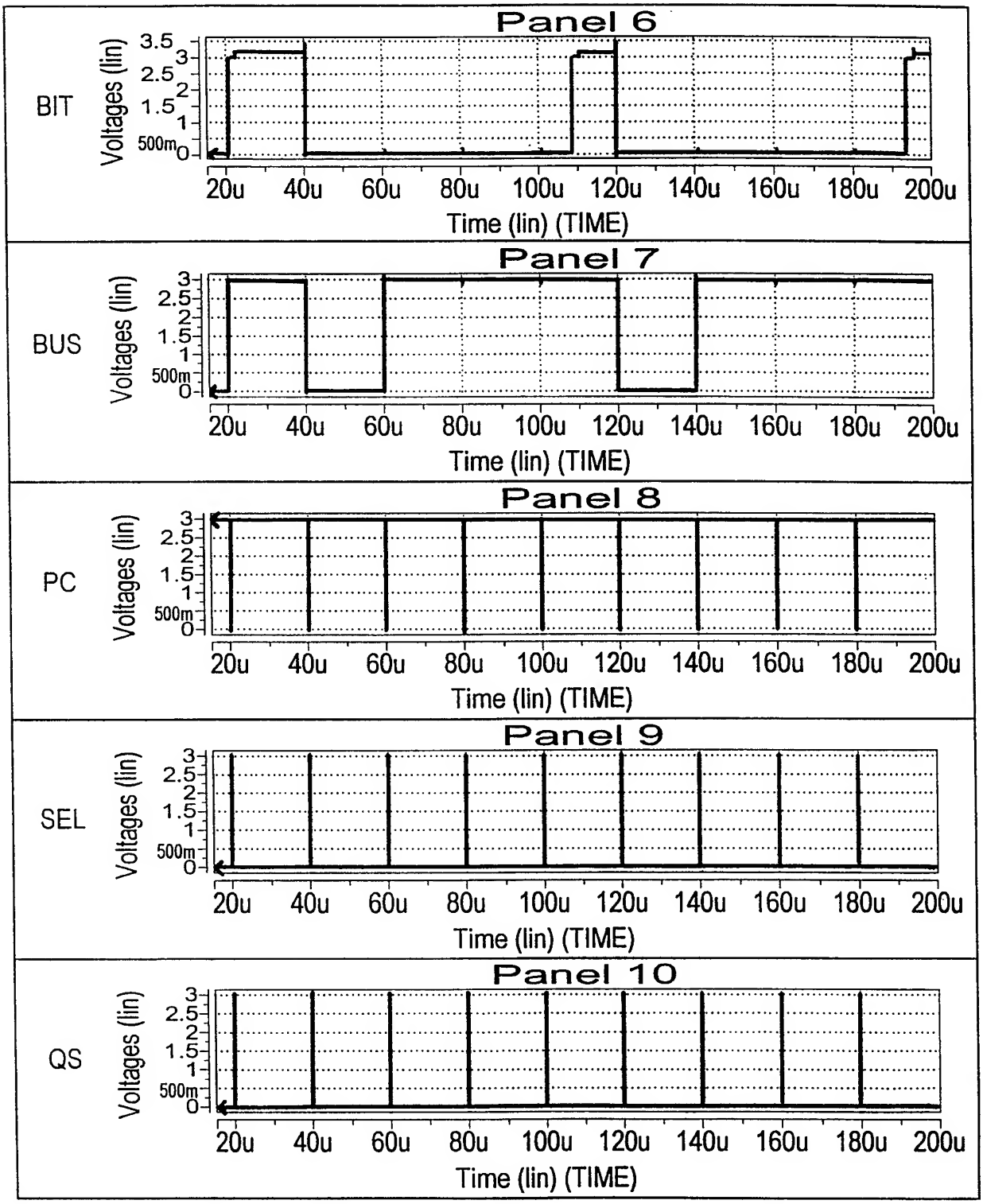
Panel 6
BIT
Voltages (lin)
3.5
3
2.5
2
1.5
1
500m
0
20u 40u 60u 80u 100u 120u 140u 160u 180u 200u
Time (lin) (TIME)
Panel 7
BUS
Voltages (lin)
3
2.5
2
1.5
1
500m
0
20u 40u 60u 80u 100u 120u 140u 160u 180u 200u
Time (lin) (TIME)
Panel 8
PC
Voltages (lin)
3
2.5
2
1.5
1
500m
0
20u 40u 60u 80u 100u 120u 140u 160u 180u 200u
Time (lin) (TIME)
Panel 9
SEL
Voltages (lin)
3
2.5
2
1.5
1
500m
0
20u 40u 60u 80u 100u 120u 140u 160u 180u 200u
Time (lin) (TIME)
Panel 10
QS
Voltages (lin)
3
2.5
2
1.5
1
500m
0
20u 40u 60u 80u 100u 120u 140u 160u 180u 200u
Time (lin) (TIME)

FIG. 4b

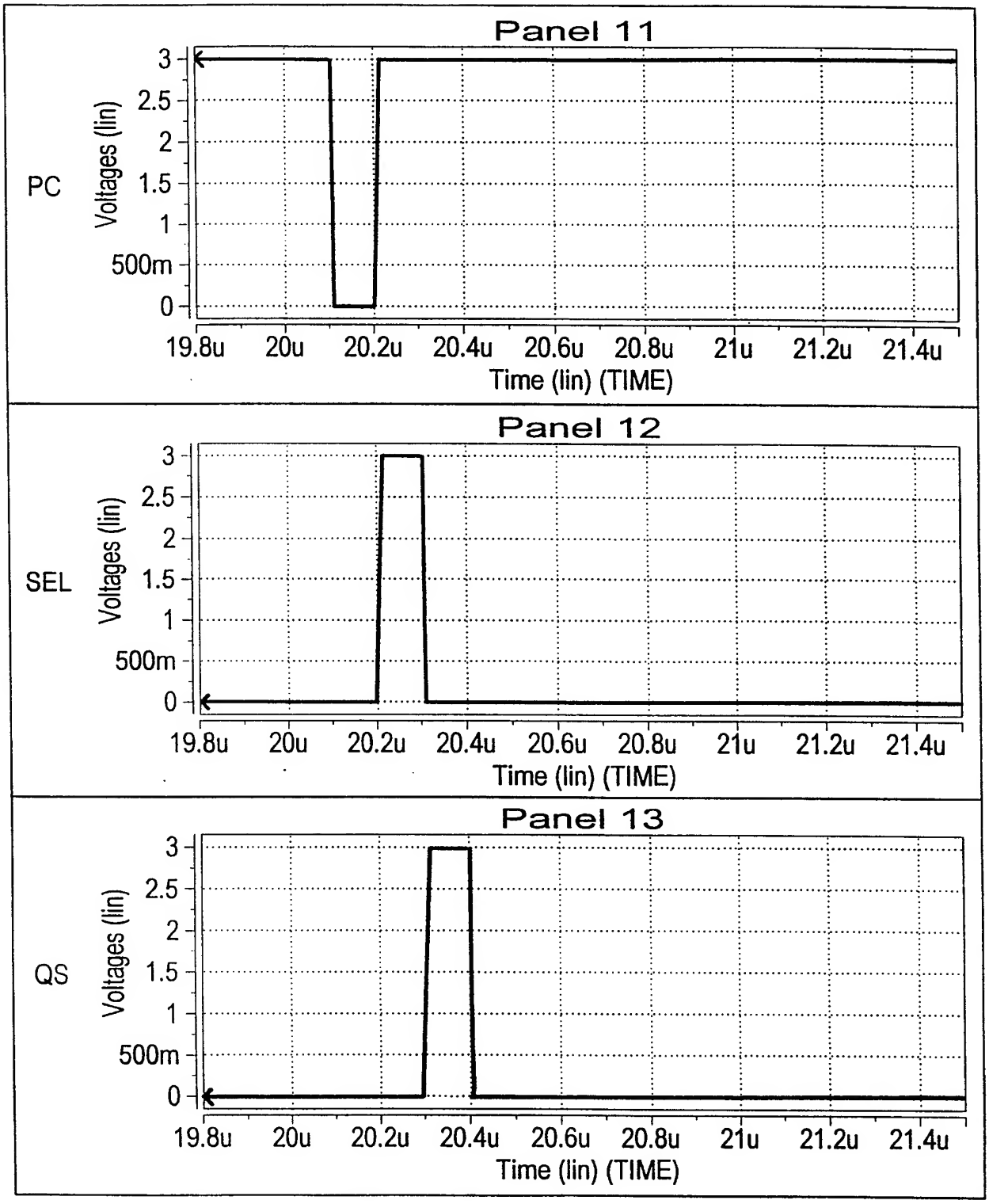
Panel 11
PC
Voltages (lin)
3
2.5
2
1.5
1
500m
0
19.8u
20u
20.2u
20.4u
20.6u
20.8u
21u
21.2u
21.4u
Time (lin) (TIME)
Panel 12
SEL
Voltages (lin)
3
2.5
2
1.5
1
500m
0
19.8u
20u
20.2u
20.4u
20.6u
20.8u
21u
21.2u
21.4u
Time (lin) (TIME)
Panel 13
QS
Voltages (lin)
3
2.5
2
1.5
1
500m
0
19.8u
20u
20.2u
20.4u
20.6u
20.8u
21u
21.2u
21.4u
Time (lin) (TIME)

FIG. 4c

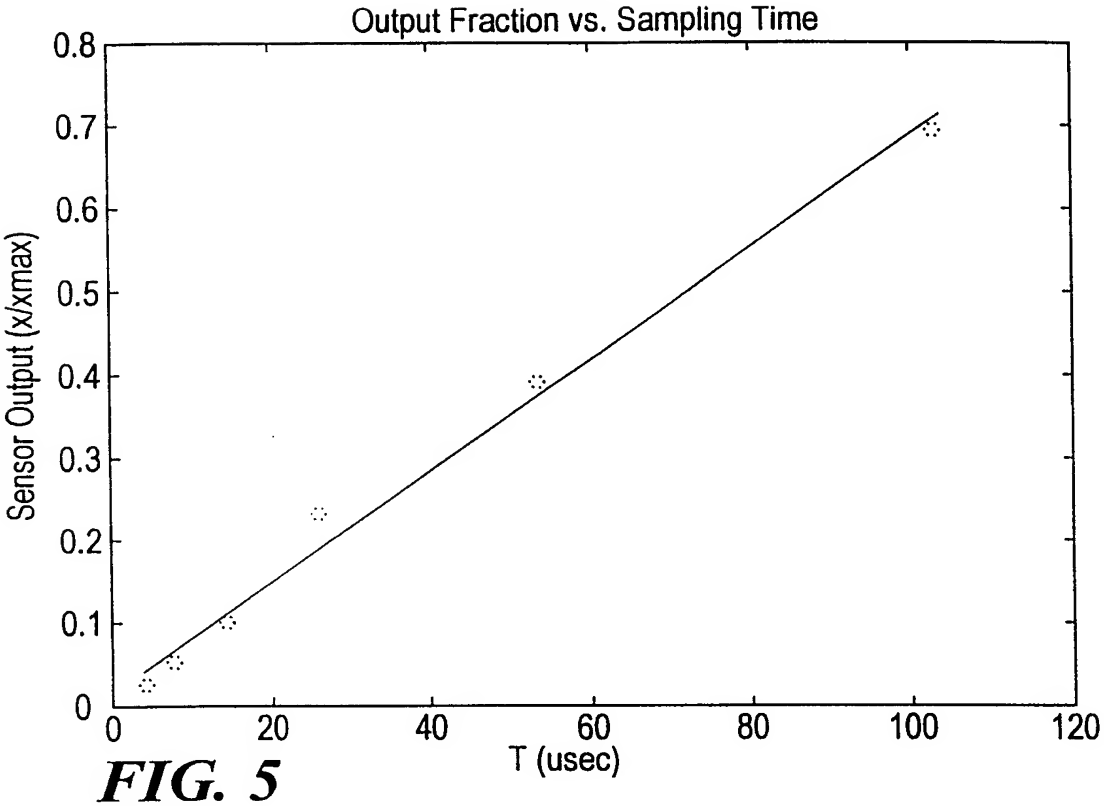
Output Fraction vs. Sampling Time
Sensor Output (x/xmax)
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
0
20
40
60
80
100
120
T (usec)

FIG. 5

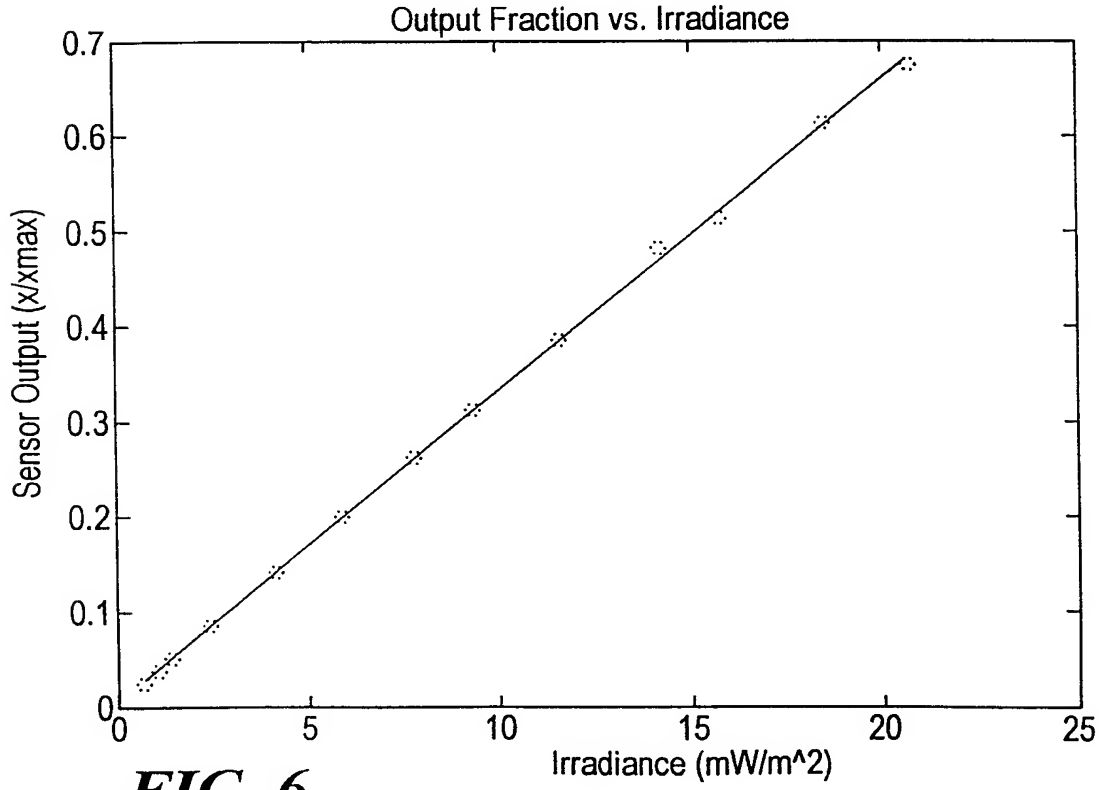
Output Fraction vs. Irradiance
Sensor Output (x/xmax)
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
0
5
10
15
20
25
Irradiance (mW/m^2)

FIG. 6

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US99/05462

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :H03M 1/10
US CL :341/143

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 341/143, 155

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

USPTO: derwent, uspat, jpo (asynchronous, delta-sigma, pixel, imager)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5,461,425 A (Fowler et al.) 24 OCT 1995 (24.10.1995), see fig. 2	1, 2
A	US 4,320,361 A (Kikkert) 16 March 1982 (16.03.1982).	1
X	van der Goes et al., Sigma-delta versus oscillator-based converter in low-cost sensor systems, 1996, IEEE, Proceedings of IEEE Instrumentation and Measureemnt Technology Conference and IMEKO Tech. Committee, vol. 2 pages 1151-1153.	1

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search 07 JULY 1999	Date of mailing of the international search report 05 AUG 1999
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